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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (Previously Presented) A contact structure of a semiconductor device, the contact structure comprising:

a dry-etchable lower conductive film;

an upper conductive film formed on the lower film and including Al or Al alloy, the upper film having edges located on the lower film;

an insulator having a contact hole exposing at least a portion of the lower film; and

an IZO layer formed on the insulator and contacting the lower film and a top surface of the upper film through the contact hole.

2. (Original) The contact structure of claim 1, wherein the contact hole exposes at least one edge of the lower film.

3. (Original) The contact structure of claim 1, wherein the distance between the edges of the lower film and the edges of the upper film is substantially uniform.

4. (Original) The contact structure of claim 1, wherein the lower film comprises Cr.

5-7. (Canceled)

8. (Previously Presented) A thin film transistor array panel comprising:

a gate conductive layer formed on an insulating substrate;

a gate insulating layer on the gate conductive layer;

a semiconductor layer on the gate insulating layer;

a data conductive layer formed at least in part on the semiconductor layer;

a passivation layer formed on the data conductive layer; and

an IZO conductive layer formed on the passivation layer,

wherein at least one of the gate conductive layer and the data conductive layer includes a dry-etchable lower film and an upper film formed on the lower film, the upper film including Al or Al alloy and having edges located on the lower film, and the IZO conductive layer contacts the lower film and a top surface of the upper film.

9. (Original) The thin film transistor array panel of claim 8, wherein edges of the lower film are located near edges of the upper film adjacent thereto.

10. (Original) The thin film transistor array panel of claim 8, wherein the IZO conductive layer contacts an edge of the lower film.

11. (Canceled).

12. (Original) The thin film transistor array panel of claim 8, wherein the distance between edges of the lower film and edges of the upper film adjacent thereto is substantially uniform.

13. (Original) The thin film transistor array panel of claim 8, wherein the lower film comprises Cr.

14. (Original) The thin film transistor array panel of claim 13, wherein the lower film has a thickness equal to or less than about 500 Å.

15. (Original) The thin film transistor array panel of claim 8, wherein the data conductive layer comprises a data line and a drain electrode separated from each other, and the IZO conductive layer comprises a pixel electrode contacting the drain electrode, a gate contact assistant contacting a portion of the gate conductive layer, and a data contact assistant contacting a portion of the data line.

16-36 (Canceled)

37. (New) The contact structure of claim 1, wherein the edges of the upper film include at least opposing edges defining the upper film in a longitudinal direction.

38. (New) The contact structure of claim 1, wherein the edges of the upper film include at least opposing edges defining the upper film in a transverse direction.

39. (New) The contact structure of claim 1, wherein the edges of the upper film include all edges defining the upper film.

40. (New) The thin film transistor array panel of claim 8, wherein the edges of the upper film include at least opposing edges defining the upper film in a longitudinal direction.

41. (New) The thin film transistor array panel of claim 8, wherein the edges of the upper film include at least opposing edges defining the upper film in a transverse direction.

42. (New) The thin film transistor array panel of claim 8, wherein the edges of the upper film include all edges defining the upper film.